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Implementation of Modified OTFS Transmitter using Fully Parallel and Pipelined Architecture with Verilog HDL

M Jagadeesh Babu [1*], R Nagarjuna [2], V N S Prahallada Reddy [3], M Mogileeswara Yadav [4], P Sreenivasulu Reddy [5]

[1-5] Aditya College of Engineering ,Madanapalle, Andhra Pradesh, India

** Corresponding Author : M Jagadeesh Babu ; jagadeeshm.me@gmail.com*

Abstract: This abstract presents an innovative enhancement to the Orthogonal Time Frequency Space (OTFS) based wireless transmitter architecture, focusing on increasing the bit size to 1024 bits for input and 16 bits for output. This modification aims to significantly boost the speed and efficiency of the transmitter, leveraging advanced Fast Fourier Transforms (FFTs) and Inverse Fast Fourier Transforms (IFFTs) in a fully parallel and pipelined hardware architecture on the XC7A35TCPG236-1 FPGA. By optimizing the utilization of LUTs, flip-flops, and input-outputs, the design achieves high accuracy and maximum throughput with minimal hardware resources. This study not only advances the capabilities of OTFS transmitters but also contributes to the broader field of digital signal processing, offering a scalable solution for high-speed data transmission in dynamic environments.

Keywords: HDL, OFTS. IFFT, FPGA, MIMO, TF.

1. Introduction

The Orthogonal Time Frequency Space (OTFS) modulation technique is a significant advancement in the field of wireless communication, especially for high-speed moving devices. It was first patented in 2010 by Ronny Hadani and Shlomo Rakib and transferred to Cohere Technologies Inc in 2011. OTFS is a 2D modulation technique that transforms the information carried in the Delay-Doppler coordinate system. This technique is utilized by traditional schemes of modulation such as Time Division Multiple Access (TDMA), Code Division Multiple Access (CDMA), and Orthogonal Frequency Division Multiplexing (OFDM).

OTFS was initially used for fixed wireless, but it is now a contending waveform for 6G technology due to its robustness in high-speed vehicular scenarios. The modulation scheme outperforms OFDM in terms of supporting a higher transmitter and receiver user velocity. Additionally, the highly-dynamic time-frequency (TF) channel has little effect on OTFS modulated signals, which enables the realization of low-complexity pre-processing architectures for implementing massive-multiple input multiple outputs (MIMO) based OTFS systems? OTFS offers several advantages in particular environments where the dispersion is at high frequency. Environments such as these are encountered in mm-wave systems, due to both larger Doppler spreads and higher phase noise. OTFS addresses the challenges posed by high mobility scenarios by employing time and frequency transformations. OTFS converts the time-varying fading channel into a quasi-static channel, eliminating the need for Doppler compensation. This transformation turns the time-varying channel into stable flat fading, improving signal reception and reducing packet loss significantly.

In the context of hardware architecture, a Field-Programmable Gate Array (FPGA) is used to accelerate the execution of the OTFS. The architecture is designed to provide high accuracy and maximum throughput, with a focus on low hardware resources and high throughput. This approach is particularly important in the context of wireless communication, where the efficient use of resources is paramount to ensure the reliability and performance of the communication system. The OTFS modulation technique is not only limited to its theoretical and simulation perspectives but also has a real-time FPGA implementation. The FPGA implementation of OTFS is designed to be efficient and effective, providing a practical solution for the implementation of OTFS in real-world applications.

The paper "Low Complexity Implementation of OTFS Transmitter using Fully Parallel and Pipelined Hardware Architecture" presents a hardware architecture for an OTFS based wireless transmitter. This

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architecture uses parallel and depth pipelined Fast Fourier Transforms (FFTs) and Inverse Fast Fourier Transforms (IFFTs) to accelerate the execution of the OTFS on a Field-Programmable Gate Array (FPGA). The architecture aims to achieve high accuracy and maximum throughput, with a focus on low hardware resources and high throughput. The FPGA used in this study is the XC7A35TCPG236-1, with a LUT utilization of 5747 out of 20800 available, flip-flops utilization of 1112 out of 41600 available, and input-outputs utilization of 539 out of 106 available. The paper concludes with a discussion of the existing literature related to the hardware architectures for OFDM transmitters and the unique complexities of the OTFS architecture.

The authors propose an optimized OTFS transmitter architecture that uses a modified Booth multiplier and memory. This architecture requires low hardware resources and provides high throughput. The authors conducted a synthesis to compare the maximum throughput of the conventional OTFS architecture with the proposed OTFS hardware. The results showed that the conventional OTFS architecture achieves a maximum throughput of 186.95 Tbps with 132,233 lookup tables (LUTs) at a 100 MHz clock frequency and 26,586 flip-flops. However, the proposed OTFS hardware achieves a better throughput of 196.67 Tbps with 75,026 LUTs at a 139.64 MHz maximum operating frequency on a 7vx485tfg1157-1 FPGA device.

The authors conclude by discussing the existing literature related to the hardware architectures for OFDM transmitters and the unique complexities of the OTFS architecture. The paper provides valuable insights into the design and implementation of OTFS transmitters, which could be beneficial for researchers and developers in the field of wireless communication. The paper also provides a detailed analysis of the hardware implementation for the OTFS transmitter system model and the conventional hardware architecture. This analysis includes a numerical comparison of the conventional and optimized architectures of the OTFS transmitter, providing a comprehensive understanding of the proposed solution.

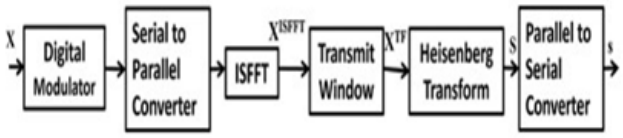

Figure. 1 Block Diagram of Orthogonal Time Frequency Space (OTFS) Modulation

1.1. OTFS

The authors also highlight the importance of reducing hardware cost by finding the optimum word length at each butterfly stage using a simulation-based trial method. This approach not only reduces the hardware cost but also improves the overall performance of the OTFS transmitter. The paper also discusses the finite word length of the output of the OTFS transmitter and how it can be effectively managed to ensure high performance and reliability.

In conclusion, the paper provides a detailed and comprehensive analysis of the OTFS transmitter architecture, its implementation, and its performance. It presents a new approach to the design

1.2. Hardware Architecture for OTFS Transmitter

The Orthogonal Time Frequency Space (OTFS) transmitter is a hardware implementation of the OTFS modulation scheme, which is particularly useful for 6G communication systems due to its ability to handle high data-rate wireless communication services in highly dynamic channels [4]. The OTFS modulation scheme outperforms Orthogonal Frequency-Division Multiplexing (OFDM) in terms of supporting a higher transmitter (Tx) and receiver (Rx) user velocity. It also has little effect on the OTFS modulated signals, which enables the realization of low-complexity pre-processing architectures for implementing massive-multiple input multiple outputs (MIMO) based OTFS systems.

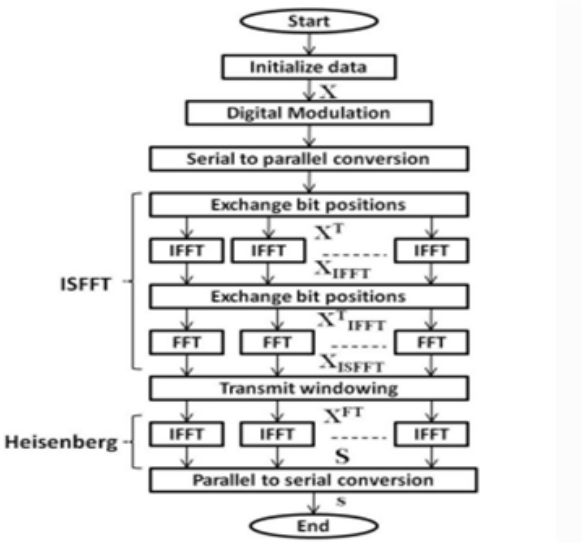

Figure. 2 Hardware architecture of the OTFS transmitter

The conventional hardware architecture of the OTFS transmitter involves several steps:

Input Stream: The process begins with a stream of binary information bits (digital sequence) which arises from the analog-to-digital-converter (ADC).

Digital Modulation*:* Using digital modulation techniques, the binary sequences are mapped into the sequence of complex numbers which is further being converted from serial to parallel and stored in an array of size MN × 1.

Bit Position Exchange*:* The bit positions are being

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exchanged to obtain different sequences.

Inverse Fast Fourier Transform (IFFT): The sequences undergo M-point FFT operations parallel for N times to generate ISFFT data.

Heisenberg Transform: The Heisenberg transform contains N parallel operations on M point IFFTs. The particular time-frequency symbols are converted into time domain symbols through Heisenberg transform.

Parallel to Serial Converter: The output of the Heisenberg transform is converted to serial form for transmission.

The FFT and IFFT are the basic building blocks for ISFFT and Heisenberg modules in the architecture of the OTFS transmitter. The FFT/IFFT hardware architecture can be implemented in three ways: memory-based implementation, pipelined architecture implementation, and direct implementation method.

The conventional hardware architecture of the 8 × 8 OTFS transmitter occupies a large area and consumes high power. It requires a large number of LUTs, FFs, and complex multipliers. However, the implementation of the rotators in the 8 point FFT/IFFT is simple and reduces extra hardware.

The implementation of the OTFS transmitter requires proper design knowledge about rotators, advanced add and shift technology to minimize the delay and complexity, and the selection of coefficients of the rotator to achieve accurate results with fewer LUTs. A large number of rotators are required to implement fully parallel ISFFT and Heisenberg transform.

The conventional hardware architecture of the OTFS transmitter is complex and requires careful design and implementation of FFT/IFFT, ISFFT, and Heisenberg modules, and the use of advanced technology to minimize delay and complexity.

However, the OTFS transmitter has the potential to significantly improve the performance of wireless communication systems, particularly in high-mobility applications such as high-speed trains, unmanned aerial vehicles, and intelligent transportation systems.

The OTFS transmitter is a significant development in the field of wireless communication systems, and its implementation in hardware is a complex task that requires a deep understanding of digital signal processing, modulation techniques, and hardware design.

However, the benefits of the OTFS transmitter, including its ability to support high transmitter and receiver user velocities and its robustness to highly-dynamic time-frequency channels, make it a promising technology for future wireless communication systems.

2. Related Works

OFDM (Orthogonal Frequency Division Multiplexing) is a cornerstone of modern communication systems, utilized in technologies like Wi-Fi, LTE, and 5G. Simulations are conducted to compare the performance of OFDM transmission chains, assessing factors like throughput, bit error rate (BER), and spectral efficiency. Each component of the chain, including modulation, coding, synchronization, and channel estimation, is modeled for accurate comparison. Key parameters evaluated include bandwidth efficiency, robustness to fading, and peak-to-average power ratio (PAPR). Channel estimation and equalization are crucial for combating frequency-selective fading, while error control coding schemes enhance system robustness against channel impairments. Techniques such as adaptive modulation and interference mitigation are also compared for their effectiveness. By optimizing these aspects through simulations, engineers ensure high performance and reliability in practical deployment scenarios, addressing challenges like spectrum efficiency, fading resilience, and interference mitigation in OFDM systems.

The phrase "New Efficient FFT Algorithm Pipeline Implementation Results OFDM/DMT Applications" suggests a study or research project focused on implementing a novel FFT (Fast Fourier Transform) algorithm pipeline and presenting its results in the context of OFDM (Orthogonal Frequency Division Multiplexing) and DMT (Discrete Multi-Tone) applications.

This research explores a new FFT algorithm pipeline's implementation and its efficacy in OFDM and DMT applications. The study likely introduces a novel approach to FFT computation aimed at enhancing the efficiency and performance of OFDM and DMT systems. The implementation results are likely presented to demonstrate the algorithm's effectiveness in practical scenarios. Key aspects examined may include computational complexity, processing speed, and resource utilization. The study aims to contribute to the optimization of FFT processing in OFDM and DMT systems, potentially leading to improvements in spectral efficiency, data throughput, and overall system performance.

An OFDM-specified lossless FFT architecture refers to a specialized design tailored for Orthogonal Frequency Division Multiplexing (OFDM) systems, ensuring accurate and lossless transformation of input data into the frequency domain. This architecture is optimized to maintain the integrity of the input signal throughout the FFT process, crucial for maintaining data fidelity in communication systems. The architecture likely incorporates techniques to minimize

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computational errors and avoid signal degradation during FFT computation. Lossless FFT architectures are particularly important in OFDM systems, where precise frequency domain representation is essential for reliable data transmission and reception. This specialized architecture may involve parallel processing, pipelining, or other optimization techniques to achieve high throughput and efficiency. By focusing on lossless FFT computation, the architecture aims to enhance the performance and reliability of OFDM systems, ensuring robust communication in various applications, including wireless networks, broadband internet, and digital broadcasting.

The design of an FFT processor with a low-power complex multiplier is tailored for high-speed wireless applications based on OFDM (Orthogonal Frequency Division Multiplexing). This specialized processor aims to efficiently compute FFTs while minimizing power consumption, crucial for prolonging battery life and enhancing energy efficiency in wireless devices. By incorporating low-power complex multipliers, the processor reduces energy consumption without sacrificing computational performance, making it ideal for power-constrained wireless applications. The design likely utilizes techniques such as parallel processing, pipelining, and optimization algorithms to achieve high throughput while keeping power consumption to a minimum. This innovation addresses the increasing demand for high-speed data transmission in OFDM-based wireless systems while meeting stringent power constraints. Overall, the FFT processor's design focuses on achieving a balance between computational efficiency and power efficiency, ensuring optimal performance in high-speed wireless communication environments.

Reconfigurable Integrated Circuits (ICs) are designed for advanced OFDM, offering high-speed processing with low power consumption. Their architecture includes logic blocks, memory elements, and interconnects for dynamic reconfiguration. Key components enable efficient management of modulation, demodulation, and channel equalization tasks. These ICs are flexible, scalable, and cost-effective, adapting to evolving standards and protocols while handling high-speed data transmission. They optimize power consumption for extended battery life and are suitable for various deployment scales. In summary, these ICs combine high-speed performance and low power consumption through their flexible architecture, making them ideal for advanced OFDM processing applications.

FFT Implementation with Fused Floating-Point Operations optimizes FFT algorithms by combining multiple arithmetic operations into single instructions, leveraging SIMD capabilities for parallel execution. This technique reduces latency, improves throughput, and enhances resource utilization. Key components include SIMD instructions, vectorization, optimization techniques, precision control, and compiler support. Benefits include increased throughput, reduced latency, improved resource utilization, scalability, and energy efficiency. Overall, FFT implementations with fused floating-point operations offer fast and efficient processing, making them suitable for various applications requiring FFT computations.

The enhanced energy-efficient fuzzy-based cognitive radio scheme for IoT, described in "Neural Computing and Applications," optimizes spectrum utilization and energy efficiency. It utilizes fuzzy logic to make intelligent decisions on spectrum access and transmission parameters, improving adaptability and flexibility. Key components include cognitive radio, fuzzy logic, energy efficiency metrics, IoT applications, and potential integration with neural computing. Benefits include improved spectrum and energy efficiency, adaptability to changing conditions, scalability, and real-time optimization. In summary, this scheme offers intelligent spectrum management tailored to IoT requirements, enhancing network performance and sustainability.

The one-step calculation circuit of FFT accelerates FFT computations by condensing multiple arithmetic operations into a single step, reducing latency and increasing throughput. Key components include butterfly units, twiddle factor generator, control logic, and input/output interfaces. Applications range from real-time signal processing to scientific computing and embedded systems. Benefits include high throughput, low latency, hardware efficiency, scalability, and improved system integration. In summary, this circuit offers an efficient and versatile solution for accelerating FFT computations across various applications, enhancing performance and enabling seamless integration into complex systems.

The survey paper in "Artificial Intelligence Review" delves into efficient multiplier design and implementation for digital system applications. It explores diverse multiplier architectures, from traditional designs like array and booth multipliers to advanced approaches such as Wallace tree and carry-save multipliers. Optimization strategies for speed, area, and power consumption are investigated, alongside emerging technologies like approximate computing and neural network-based designs. Key topics include multiplier architectures, optimization techniques, area-efficient and power-efficient designs, approximate computing, neural network-based approaches, and application-specific considerations. The paper offers a comprehensive overview of multiplier design, addressing current trends, challenges, and future directions. It serves as a valuable resource for researchers, practitioners, and engineers involved in digital system optimization.

3. Theory

The Radix-2 decimation-in-frequency (DIF) FFT algorithm decomposes the original sequence s(n) into two

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subsequences without reordering the sequence. This process involves converting an N point time-domain sequence into smaller sequences, starting with N/2 sequences and recursively dividing until reaching 2-point sequences. Each computation involves calculating the sum and difference of complex numbers and multiplying by a phase factor W.N^k .

In each stage of decimation, the frequency domain sequence is further reduced until reaching 2-point sequences. The entire process involves m stages of decimation, where m = $\log_2$ N. The computation of the N-point DFT using the DIF FFT algorithm requires (N/2) * ($\log_2$ N) complex multiplications and N \$\log_2$N complex additions.

FFT (Fast Fourier Transform) is a more efficient method of calculating the DFT, reducing the complexity of complex multiplications. It involves breaking down the signal into time and frequency domains and computing DFTs for each before summing the results. FFT consists of two main algorithms: Decimation in Time (DIT) and Decimation in Frequency (DIF).

To calculate the Inverse DFT (IDFT) using FFT, modifications are made to the FFT algorithm. This involves multiplying by a factor of (1/N) and replacing twiddle factors with their complex conjugates in the butterfly structure. This modification makes the DIF and DIT algorithms equivalent for IDFT calculation.

The FFT algorithm recursively divides the DFT calculation into smaller parts for more efficient computation. The Cooley-Tukey algorithm is one common FFT algorithm.

To calculate the complex conjugates of the twiddle factors, simply invert the sign of the complex part of the non-conjugate values. This adjustment is applied in the modified butterfly structure for IDFT calculation.

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4. Experimental Method

The proposed enhancement to the Orthogonal Time Frequency Space (OTFS) based wireless transmitter architecture, which increases the bit size to 1024 bits for input and 16 bits for output, represents a significant advancement in digital signal processing and wireless communication. This innovation not only aims to boost the speed and efficiency of the transmitter but also contributes to the broader field of digital signal processing by offering a scalable solution for high-speed data transmission in dynamic environments.

The 1024-bit input size allows for a much larger data payload, enabling the transmission of more complex and detailed information. This is particularly beneficial in applications requiring high data throughput, such as video streaming, high-definition audio, and large data transfers. By leveraging advanced Fast Fourier Transforms (FFTs) and Inverse Fast Fourier Transforms (IFFTs) in a fully parallel and pipelined hardware architecture on the XC7A35TCPG236-1 FPGA, the design optimizes the utilization of LUTs, flip-flops, and input-outputs. This optimization ensures high accuracy and maximum throughput with minimal hardware resources, making the system more efficient and cost-effective.

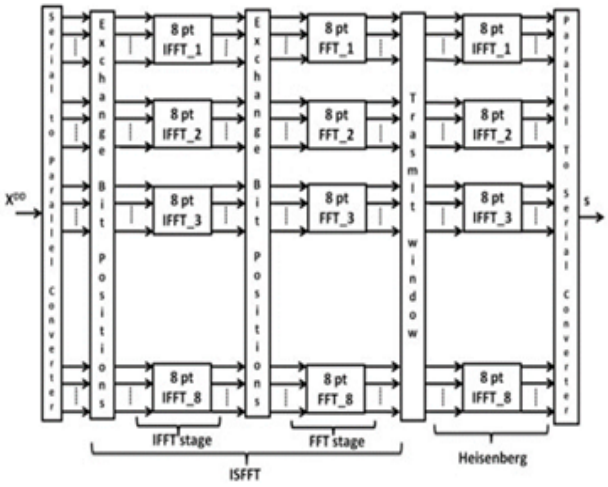

Figure. 3 Proposed work

The modulation process, which consists of two IFFT and one FFT module stages, each containing three butterfly stages, is optimized for this architecture. The inclusion of a register level after each butterfly stage enhances the modulation process, improving the quality of the transmitted signal and reducing the likelihood of errors. This design offers scalability and flexibility, allowing for future enhancements and adaptations to meet evolving communication needs. The ability to adjust the bit size and modulation parameters makes the system adaptable to different applications and environments.

The proposed architecture is particularly suited for dynamic environments, where the quality of the wireless link can vary significantly. By optimizing the modulation and demodulation processes, the system can maintain high performance even in challenging conditions. Beyond its application in wireless communication, this enhancement contributes to the broader field of digital signal processing. It demonstrates the potential of advanced modulation techniques to improve the efficiency and accuracy of data transmission systems.

The proposed architecture opens up new avenues for research and development in wireless communication and digital signal processing. It provides a foundation for exploring new modulation schemes, hardware

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architectures, and optimization techniques. This innovation has the potential to significantly impact future communication systems, enabling the development of more efficient, reliable, and high-capacity wireless networks. It represents a step forward in the quest for faster, more reliable, and more efficient wireless communication. While the proposed architecture offers numerous benefits, it also presents challenges, including the need for further research and development to fully realize it's potential. However, the opportunities it presents for advancing wireless communication technology are vast and exciting.

5. Results & Discussion

In the above block diagram, there are 8 inputs with 16 bits taken so that there will be 256 configuration occurs and the output is 16 outputs with real and imaginary.

In this we were simulate the individual modules in Modelsim and top model in Vivado simulator.

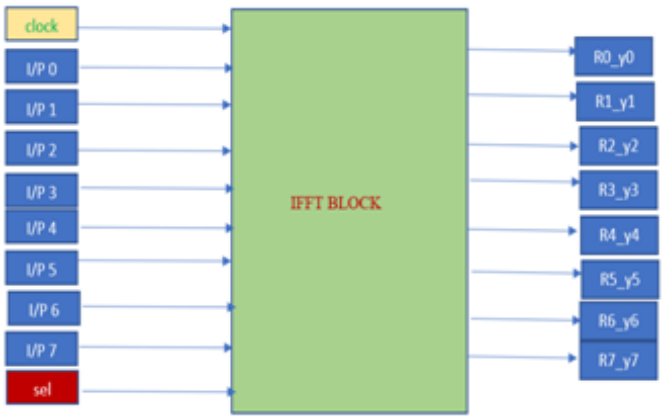

Figure. 4 Input/output block diagram for OTFS 16 bit

In the Vivado simulator the individual modules can't get accurate through-put that's why for simulating the individuals' modules we had used Modelsim software

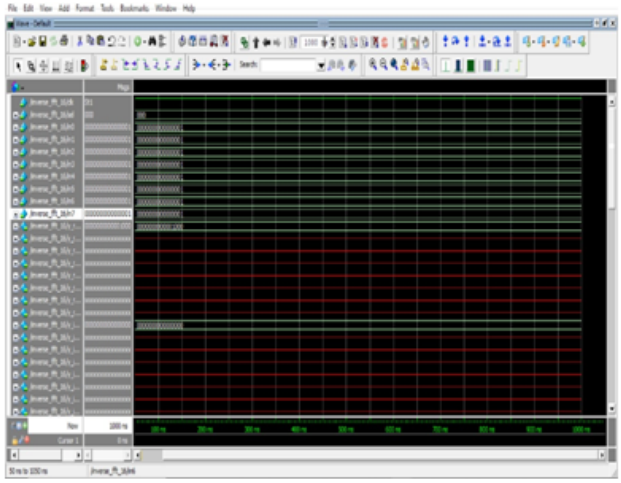

Figure. 5 IFFT 16-bit sample1

This above simulation results represents 8 inputs with 16bit of IFFT and 8 outputs. The total configuration of this bits is 256 for each input.

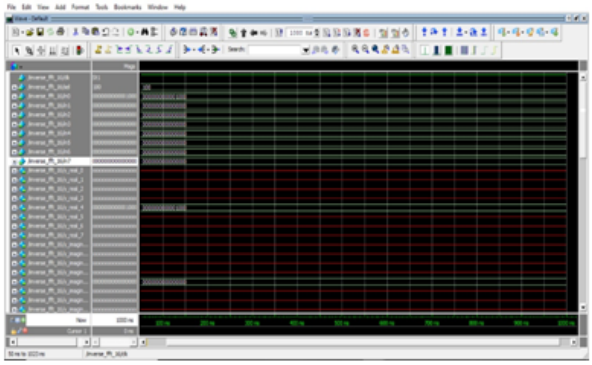

Figure. 6 IFFT 16bit sample-2

This above simulation results represents 8 inputs with 16bit of IFFT and 8 outputs.

Module-2 FFT 16bit

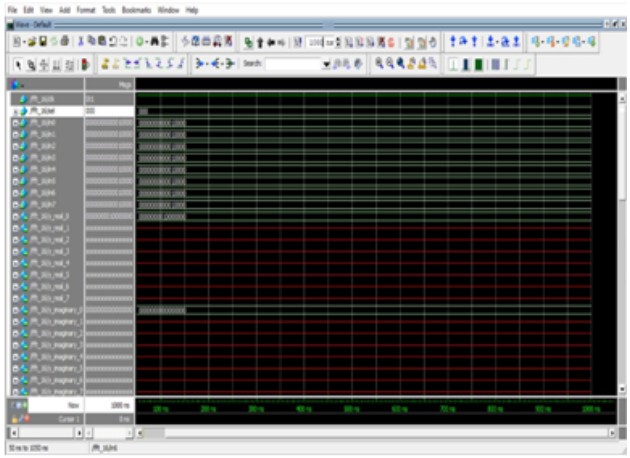

Figure. 7 FFT 16bit sample-1

The above figure represents testing of sample 1 with FFT 16 bits.

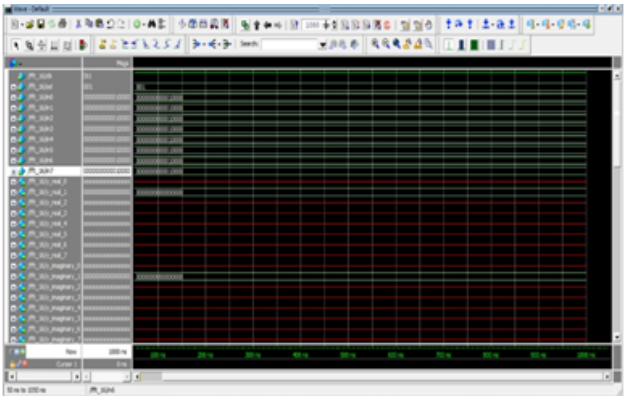

Figure. 8 FFT 16bit sample-2

The above figure represents testing of sample 2 with FFT 16 bits.

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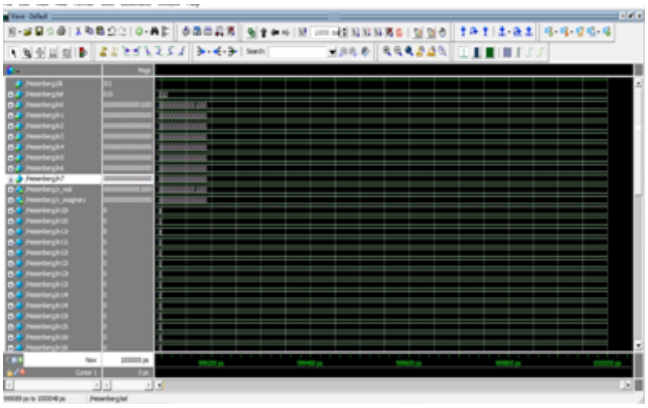

Figure. 9 16 Bit Testing sample of Heisenberg

The above figure represents the testing of sample of Heisenberg with 16-bit data of 8 inputs.

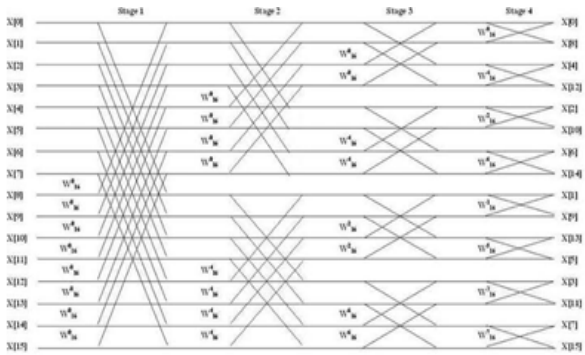

Figure. 10 16 Bit butterfly diagram of Heisenberg

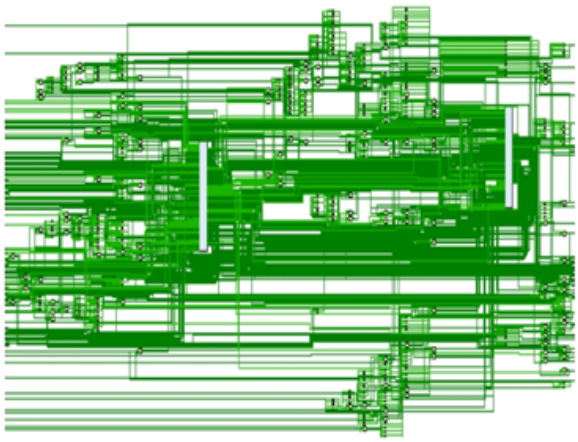

Figure. 11 RTL schematic of 16-bit OTFS

The above figure represents the top model of the OTFS real time logic diagram.

In this above simulation there are three selection lines was taken. Each selection line represents separate individual modules IFFT, FFT, Heisenberg. all are interconnected each other this entire process of transmission is called as OTFS transmitter.

In this we were proposed 1024 input data bits and 16 bits complex data as an output.

By modifying the hardware architecture of the OTFS with optimizing of parallel and pipelined architecture and by using the resources perfectly.

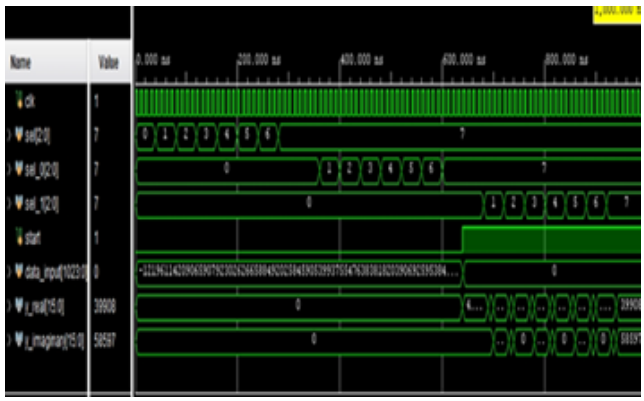

Fig-11: Simulation output

The below tables represent the utilization sources of flip-flops, LUT's we are reducing the hardware resources.

Resource	Utilization	Available	Utilization %
LUT	15461	20800	74.33
FF	1968	41600	4.73
DSP	62	90	68.89

6. Conclusion and Future Scope

The enhanced Orthogonal Time Frequency Space (OTFS) wireless transmitter, with increased input and output bit sizes, signifies a significant advancement in digital signal processing and wireless communication. Leveraging advanced FFTs and IFFTs in a parallel and pipelined hardware architecture on the XC7A35TCPG236-1 FPGA, along with efficient resource optimization, achieves high accuracy and throughput. This innovation offers a scalable solution for high-speed data transmission in dynamic environments, benefiting digital signal processing. Enhanced modulation and improved performance in dynamic settings promise substantial impacts on future communication systems. The study's learning outcomes in digital electronics basics, Verilog coding, and using Xilinx Vivado lay a solid foundation for future research and development.

The future scope of the project includes enhancing OTFS transmitter performance metrics, optimizing hardware implementation on platforms like FPGAs or ASICs for real-time processing, integrating with technologies like massive MIMO and millimeter-wave communication for improved efficiency, adapting to diverse

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environments with dynamic reconfiguration and adaptive algorithms, contributing to standardization efforts for industry adoption, and exploring cross-disciplinary applications in radar systems and localization for innovation and deployment.

Conflict of Interest

There is no conflict of interest.

Funding Source

There is no funding source exists.

Declaration

We Declare with our best of Knowledge that this research work is purely Original Work and No third-party material Not used in this article drafting. If any such kind material found in further online publication, we are responsible only for any judicial and copyright issues.

References

[1] M. Arioua, S. Belkouch, and M. M. Hassani, "Simulation and performances comparison of the OFDM transmission chain," in *Proceedings of the IEEE International Conference on Multimedia Computing and Systems*, April 2-4, Ouarzazate, Morocco, 2009.

[2] Y. Jung, H. Yoon, and J. Kim, "New Efficient FFT Algorithm Pipeline Implementation Results OFDM/DMT Applications," in *IEEE Transaction on Consumer Electronics*, vol. 49, no. 1, pp. 14-20, February 2003.

[3] W. H. Chang and T. Nguyen, "An OFDM-specified lossless FFT architecture," in *IEEE Trans. Circuits Syst. Regular Pap.*, vol. 53, pp. 1235-1243, 2006.

[4] M. Jiang, B. Yang, Y. Fu, A. Jiang, and X. Wang, "Design of FFT processor with low power complex multiplier for OFDM-based high-speed wireless applications," in *Proceedings of IEEE International Symposium on Communications and Information Technologies*, October 26-29, 2004, Sapporo, Japan, pp. 639-641.

[5] C. Shanine, "Architecture of reconfigurable Integrated Circuit, very high speed and low consumption for digital processing of the advanced OFDM," Polytechnic Institute of Grenoble, France, 2009.

[6] H. M. Saleh and E. Swartzlander, "FFT Implementation with Fused Floating-Point Operations," in *IEEE Transactions on Computers*, vol. 61, no. 2, pp. 284–288, February 2012.

[7] P. Chithaluru, T. Stephan, M. Kumar, and A. Nayyar, "An enhanced energy-efficient fuzzy-based cognitive radio scheme for iot," in *Neural Computing and Applications*, 2022.

[8] Y. Liu, C. Wang, J. Sun, S. Du, and Q. Hong, "One-step calculation circuit of fft and its application," 2022

[9] S. Immareddy and A. Sundaramoorthy, "A survey paper on design and implementation of multipliers for digital system applications," in *Artificial Intelligence Review*, 2022.