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Performance Trade-offs in RF Design: A Comprehensive Analysis of Double Balanced Gilbert Cell Mixer

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Abstract: Designers of RF (Radio Frequency) circuits must exercise caution throughout the different phases of system design. Prior to implementation, a comprehensive examination of trade-offs inherent in RF system design, encompassing factors such as power, supply voltage, noise, linearity, gain, and frequency considerations, is essential. This paper delves into a simulation-based analysis using Advanced Design Systems (ADS), exploring various parameter combinations to grasp their impact on overall system performance. Focusing on a critical component, the RF mixer, in the receiver front end, evaluation is conducted across different VLSI (Very Large-Scale Integration) process nodes and design parameters to comprehend the relationship between numerous performance metrics including conversion gain, noise figure, third order intercepts, and compression points. The insights garnered from this study offer strategies to enhance RF design parameters to achieve desired performance characteristics.

Keywords: RF mixer design, linearity, conversion gain, noise, multi-frequency band approach, Performance Evaluat

1. Introduction

Decades of RF and microwave theory research, along with nearly thirty years devoted to RF IC (Integrated Circuit) research, haven't mitigated the significant hurdles in designing RF circuits and transceivers. These challenges stem from the diverse disciplines within RF design, demanding a deep understanding of seemingly unrelated fields, necessitating a solid foundational background. RF circuits and transceivers face trade-offs outlined in the RF design hexagon as shown in Figure 1, such as sacrificing power consumption or linearity to improve amplifier noise performance. Meeting the demands for optimal performance, cost-efficiency, and functionality presents continuous challenges. Designers aim to support multiple transceivers across diverse frequency bands for wireless standards like Wireless-Fidelity (Wi-Fi), Bluetooth, and Global Positioning System (GPS), etc. This paper evaluates design trade-offs for a down-conversion double-balanced RF mixer. Wireless Access Systems (WAS) are vital across applications, requiring stringent performance standards in cost, power, and size. Adoption of recent Wireless Local Area Network (WLAN) standards like 802.11ax is crucial, especially in public Wi-Fi projects, optimizing the 5 GHz band. Internet Protocol (IP) technologies like Voce Over Long Term Evolution (Vo-LTE) and Voice Over Wireless-Fidelity (VoWi-Fi) demand integrated governance for multimedia services, reducing end-user costs.

Upgrading wireless transceiver structures is essential for future demands. The RF mixer translates frequencies as shown in Figure 2, serving as either a downconverter or upconverter [2]. Its vital role spans entertainment, communication, testing, radar systems, etc. RF mixers are evaluated based on several key performance parameters like linearity, noise figure, and conversion gain. Conversion gain reflects the mixer's efficiency in

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amplifying and converting RF input signals to the desired frequency output, while noise figure indicates its noise performance.

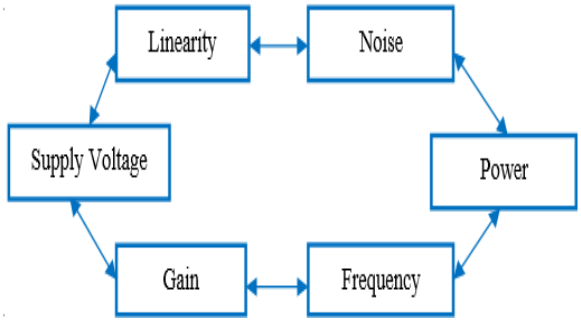

Figure 1. RF design trade-offs - Hexagon [1]

Linearity in RF mixers is vital for signal fidelity and is evaluated through metrics like third-order intercept point (IP3) and gain compression, indicating the onset of nonlinear behaviour and the point where gain starts to decrease respectively.

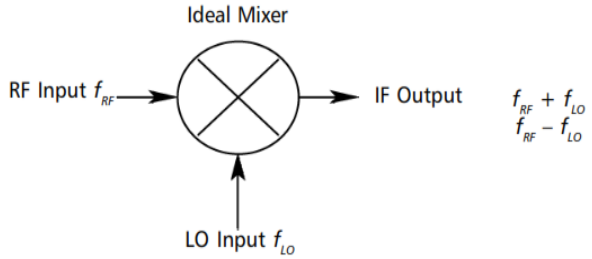

Figure 2. Ideal mixer - typical frequency mixing process

The paper is structured as follows: Section 2 reviews relevant literature, Section 3 outlines mixer design methodology, Section 4 covers experimental process, followed by results and discussion in Section 5, and Section 6 concludes with inferences and future scope.

2. Related Work

This survey covers numerous literary works on RFIC design trade-offs, exploring performance metrics, circuit architectures, and optimization techniques.

Douss et al. discuss RF CMOS circuit design trade-offs and optimization techniques for power, gain, and linearity for multiple standards [3].

Satyanarayana et al. describe the design flow for a double balanced gilbert cell mixer in a 130 nm process node for simultaneous enhancement of performance metrics [4]. Behzad Razavi articulates trade-offs in RF CMOS (Complementary Metal Oxide Semiconductor) power amplifier design [5].

Kumar et al. brief trade-offs in low-noise amplifier (LNA) design for RF various applications [6].

Avvaru S et al. discuss gain enhancement techniques and more linear RF mixer design for ultra-low power (ULP) wireless systems [7].

Dixit et al. present trade-offs in RF front-end design for multi-standard receivers [8]. E.A. Ball explores trade-offs in RF mixer design, emphasizing gain, linearity, and noise balance, etc. performance parameters [9].

Ravinutala et al. critically study Gilbert cell topology-based active mixers and performance metrics mitigation [10].

Wang et al. highlight internal design trade-offs in passive and active mixer architectures [11].

Padaki et al. discuss techniques for suppressing LO leakage in RF mixers and their impact on system performance in full-duplex communication systems [12]. Additionally, recent work focuses on improving RF mixer performance with inductive peaking and degeneration techniques for RLAN and LP-WAS [13]. This paper extends beyond previous works by targeting various technology/process nodes, mixer design methodology, and multi-frequency band approaches, addressing MOSFET operating conditions and simulation matching with design to draw inferences on various performance metrics.

3. Design Methodology

The Gilbert cell double balanced down-conversion active mixer relies on current switching, with resistive loads based on transistor states (M3-7) as shown in Figure 3.

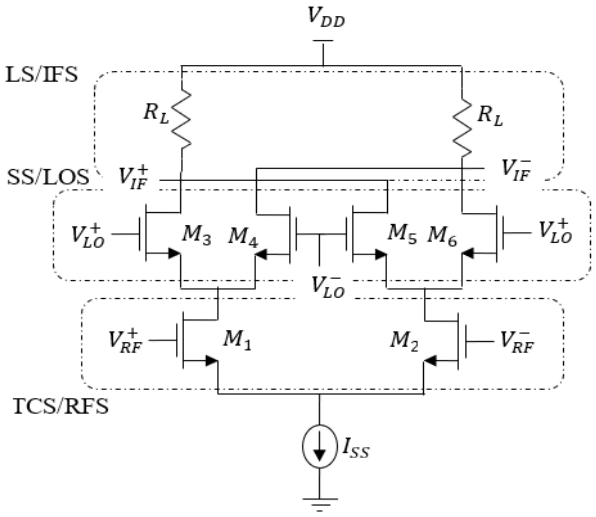

Figure 3. Stacked Gilbert cell double balanced differential RF active mixer

It consists of three stages: RF Transconductance Stage/Radio Frequency Stage (TCS/RFS) as a voltage-to-current converter, Switching Stage/Local Oscillator Stage

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(SS/LOS) as a current switching block, and Load Stage/Intermediate Frequency (LS/IFS) as a current-to-voltage (I-V) converter, forming a stacked mixer stage topology. The mixer yields an IF output proportionate to the product of LO and RF input currents.

The mixer yields an IF output proportionate to the product of LO and RF input currents. It employs differential RF and LO signals for noise tolerance in comparison with that of the single ended inputs.

4. Experimental Procedure

The design flow estimates experimental design parameters, including device dimensions, for the double balanced mixer.

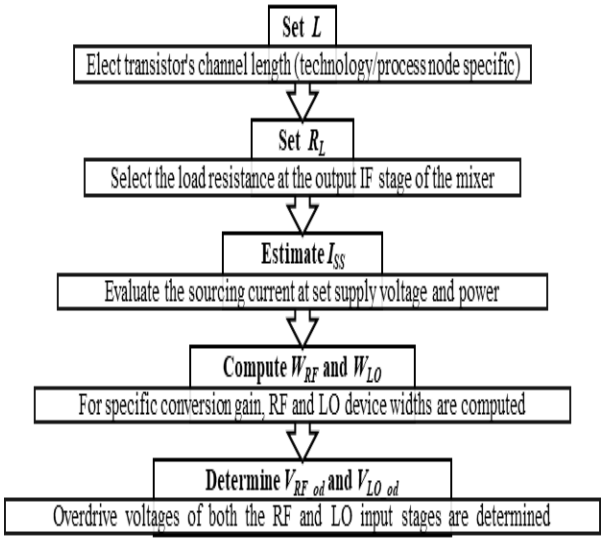

Figure 4. Design flow of the conventional mixer

By using the Eq. (1) – (3) an estimation of different design parameters for transistors shown in Fig. 3 are computed.

Mixer's conversion gain,

$$A_v \approx \frac{2}{\pi} g_m R_L \quad (1)$$

Current through the transconductors, $I_{ds} = \frac{{g_m}^2 L}{2\mu_n C_{ox} W}$ (2)

The transconductance of the transistors, $g_m = \frac{2I_{ds}}{(V_{GS}-V_T)}$ (3)

Table 1. License free frequencies for wireless systems in India [14]

Range of Frequencies	Application specific Wireless equipment
2400 - 2483.5 MHz	Equipment with low power
5725 - 5875 MHz	Low Power Wireless Access Systems (LP-WAS) - Radio LAN / Wireless LAN

A multi-frequency band approach is proposed for comprehensive design validation. Table 1 outlines various frequency ranges that can be used for both RF and local oscillator inputs to achieve a down-converted output intermediate frequency of 100 MHz.

The mixer specifications outlined in Table 2 are crucial for the design process. This design is tailored for the 130 nm CMOS technology node, and identical specifications are applied to the other nodes (180 nm) discussed in this paper, using the previously described equations and mixer specifications.

Table 2. Mixer specifications and computed design parameters

Parameter	Value
Supply voltage, V_{DD}	1.3 V
D.C Power, $P_{d.c}$	< 5 mW
Conversion gain, *CG*	> 10 dB
Noise figure (SSB), *NF*	< 10 dB
Third order input intercept,	> -10 dBm
1-dB gain compression, *1-dB*	> -15 dBm
Transistors Gate length, *L*	0.13 µm
TCS/RF transistors Width, W_{RF}	130 µm
SS/LO transistors Width, W_{LO}	65 µm
Mixer's Current source, I_{SS}	2 mA
IF output Load resistance, R_L	500 Ω
RF overdrive voltage, V_{RF_OD}	60 mV
LO overdrive voltage, V_{LO_OD}	120 mV

5. Results and Discussion

The mixer design is simulated using Advanced Design Systems (ADS) software, for high frequency and high speed applications [15]. Inputs of 1 µW RF power and 1 mW LO power (-30 dBm and 0 dBm respectively) with a 50 Ω source resistance are applied, and the output IF signal is observed for a 500 Ω load resistance.

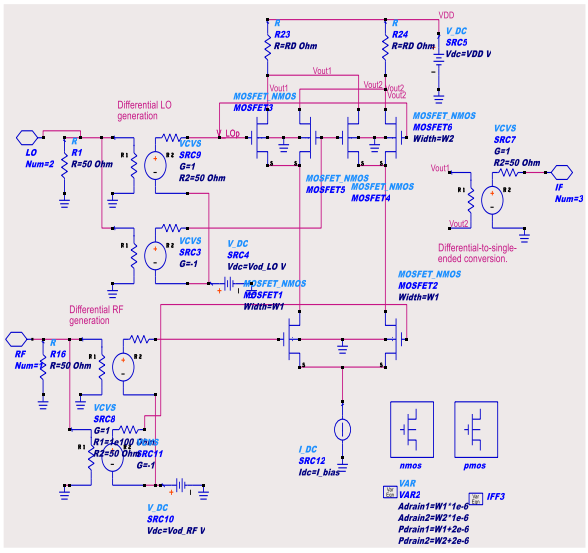

Figure 5. Gilbert cell mixer schematic in ADS using 130 nm CMOS model files

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5.1. Design and Simulation Match

MOSFET operating points are validated and matched with transistor operation in saturation.Relationships between overdrive voltage and V_{ds}, threshold voltage and V_{gs}, and drain saturation voltage V_{ds} are given from Eq.(4) to (6) [16].

$$(V_{ds} \geq V_{RF\_od})_{M1-2}, (V_{ds} \geq V_{LO\_od})_{M3-6} \quad (4)$$

$$(V_{gs} \geq V_{th})_{M1-6} \quad (5)$$

$$(V_{ds} \geq V_{dsat})_{M1-6}, (V_{ds} \geq V_{gs} - V_{th})_{M1-6} \quad (6)$$

5.2. Mixer Simulation for Gain, Linearity and Noise

For accurate simulation, highest-order mixing product is set. Lower orders speed up simulations but may sacrifice accuracy, warranting testing for significant result changes with increased harmonics or order.

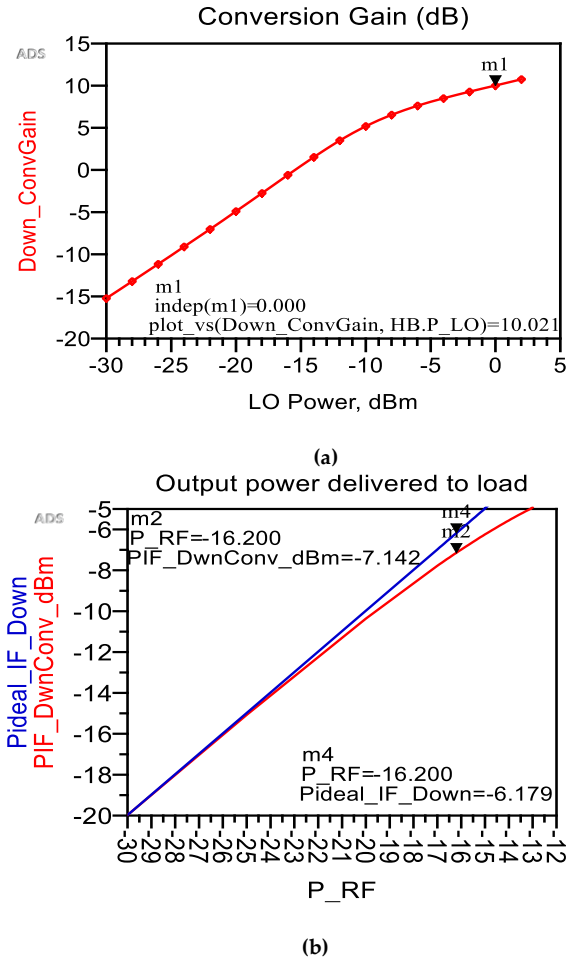

Figure 6. Mixer Simulation
(a) Down conversion gain vs. LO powers (b) 1 dB gain compression at -16.22 dBm RF power

Gain compression characterization determines the signal amplitude a mixer can handle before significant distortion occurs. By sweeping input signal power levels, the conversion gain is reduced by 1 dB from its small-signal value, at an RF input power level of -16 dBm, noticeable gain compression of 1 dB occurs.

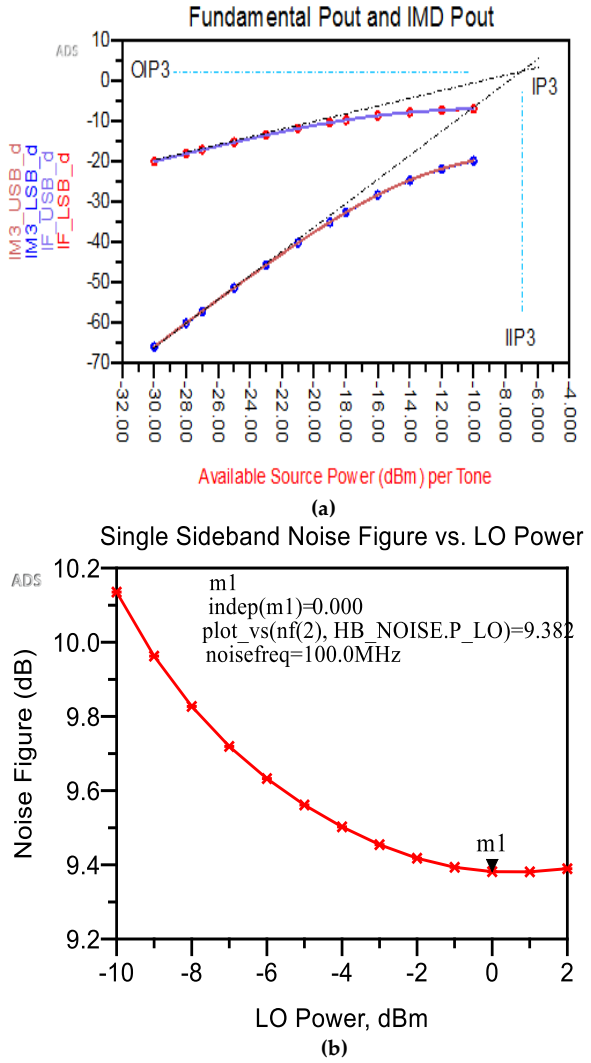

Figure 7. Linearity and noise performance
(a) Intercepts IIP3 and OIP3 graph (b) SSB noise figure with LO power

Near -7 dBm, the extrapolated 3rd order intermodulation and IF output curves converge, indicating the IP3 point, as determined by the Harmonic Balance controller component using the setup shown in Figure 7.

5.3. Formulation of Figure of Merit of the Mixer

The double balanced down-conversion mixer's performance is evaluated using a benchmark figure of merit [17], incorporating key metrics: input RF frequency, conversion gain, single sideband noise figure, input LO power, DC power, and input intercept point.

$$FoM = 10log\left[\frac{10^{(CG-2NF_{SSB}+IIP3-10-P_{LO})/20} f_{RF}/1\ KHz}{P_{d.c}/1\ mW}\right] \quad (7)$$

5.4. Mixer Validation using Multi-frequency Band Approach

The double balanced down-conversion Gilbert cell mixer design is simulated across various frequency bands in a 130 nm CMOS process node, using the design parameters described in Table 2. Results show a conversion gain just over 10 dB and a single sideband noise

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figure below 10 dB, meeting specifications. However, linearity performance is inadequate, with input intercept points below 0 dBm and 1-dB compression points exceeding -15 dBm. The design is also simulated in 180 nm technology node for result reliability.

Table 5. Simulation results of the down conversion mixer, 130 nm process node

Performance Metric	f_{RF} = 2400 MHz	f_{RF} = 5825 MHz
Conversion Gain, *CG* (dB)	10.89	10.01
1-dB gain compression	-15.99	-16.22
SSB noise figure, NF_{SSB} (dB)	9.27	9.38
3rd order input intercept, *IIP3*	-6.71	-7.1
Figure of Merit, *FoM* (dB)	52.66	51.72

Table 5 illustrates that as frequency increases, maintaining similar performance metrics deteriorates the final figure of merit (*FoM*) for the mixer, even for the same 130 nm CMOS processing node.

5.5. Validation of Mixer at different processing nodes

Mixer design is carried out in 180 nm and 130 nm process nodes at 1.8 V and 1.3 V supply voltages respectively, and used multi frequency band approach also.

Table 6. Performance of mixer for different nodes, supply voltages, frequencies

Process node	V_{DD} (V)	f_{RF} (MHz)	*FoM* (dB)
180 nm	1.8	2400	48.34
130 nm	1.3	5825	50.75

Inference can be drawn from the table that with miniaturized nodes, lower supply voltages and at higher input frequencies, overall *FoM* of the mixer got enhanced.

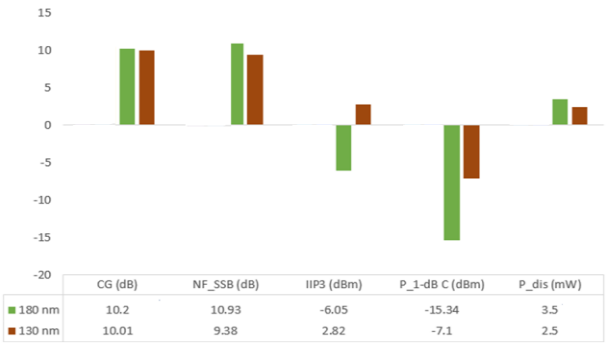

Figure 8. Visualization of mixer performance in various CMOS process nodes

Figure 8 shows that as technology advances and RF and LO frequencies increased to maintain consistent performance; DC power significantly decreases. This suggests a likely improved performance and in turn the final *FoM* of the designed mixer.

6. Conclusion and Future Scope

A down-conversion double balanced Gilbert cell RF mixer is designed and simulated for metrics like conversion gain, linearity, and noise figure across various process nodes and RF frequencies using ADS. Advancements in technology nodes (from 180nm to 130 nm) improve performance metrics due to smaller feature sizes and transistor performance. However, all metrics may not always improve and some may get degrades at specific frequencies. Technology advancements can enhance conversion gain and reduce power consumption through optimized circuit design and supply voltage scaling. Careful consideration of design metrics is crucial for maximizing benefits. with ongoing advancements in technology nodes enhancing noise figure while necessitating innovative approaches to address potential linearity challenges, particularly at specific frequencies. Optimized circuit design parameters, including supply voltage scaling and careful consideration of transistor dimension, is crucial for maximizing conversion gain and minimizing power consumption. Additionally, future developments may focus on further miniaturization, integration, and support for multi-band and wideband operation to meet the demands of modern communication systems.

Conflict of Interest

Authors declare that they do not have any conflict of interest.

Authors' Contributions

Dr.Avvaru Subramanyam researched literature, conceived the study, modelled, and simulated. Dr. RVS Satyanarayana involved in data analysis. Dr. C. Pakkiraiah wrote the first draft of the manuscript. Dr. L Bhargava Kumar revised the first draft of the manuscript with suitable inclusions. Dr. P. Gangadhara Reddy did mathematical computations. Mr. P. Venkateswarlu 6 checked for feasibility of the method involved. All authors reviewed and edited the manuscript and approved the final version of the manuscript.

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Declaration

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References

[1] Behzad Razavi, "RF Microelectronics", 2nd Edition, Prentice Hall, India, pp. **3-4**, **2012**. ISBN 978-0-13-713473-1

[2] Hank Zumbahlen, "Basic Linear Design", Analog Devices, Ch.**4**, **2007**.

[3] Douss S, Touati F and Loulou M (2007), "Design Optimization Methodology of CMOS Active Mixers for Multi-Standard Receivers", World Academy of Science, Engineering and Technology, International Journal of Electronics and Communication Engineering, Vol. **1**, No. **9**, pp. **1328-1336**, **2008**.

[4] SRVS, Avvaru S, "Design and optimization of double balanced gilbert cell mixer in 130 nm CMOS process," Solid State Electronics Letters, Vol. **2**, pp.**129–139**, **2020**.

[5] B. Razavi, "Challenges in portable RF transceiver design," IEEE Circuits and Devices Magazine, vol. **12**, no. **5**, pp. **12-25**, **296**.

[6] Kumar Ravinder, Kumar Munish, Srivastava Viranjay. "Design and Noise Optimization of RF Low Noise Amplifier for IEEE Standard 802.11A WLAN," International Journal of VLSI Design & Communication Systems, Vol. **3**, **2012**.

[7] Avvaru Subramanyam, R.V.S. Satyanarayana, "Improved Conversion Gain with High SFDR and Highly Linear RF Mixer using Inductive Gate Biasing Technique for Low Power WAS and Radio LAN Applications," ICMEET-22, Bhimavaram, Springer, **2022**.

[8] Y. R. Dixit and S. Muhammed, "Performance Trade-offs of a Software Defined Radio for 2G and 3G Cellular Mobile Communication Standards," International Conference on Communication Systems, Delhi, **pp. 1-5**, **2006**.

[9] E. A. Ball, "Investigation into the Relationship Between Conversion Gain, Local Oscillator Drive Level and DC Bias in a SiGe Transistor Transconductance Modulated Mixer at 24-28 GHz," IEEE Texas Symposium on Wireless and Microwave Circuits and Systems (WMCS), Waco, TX, USA, pp. **1-6**, **2021**.

[10] Avvaru Subramanyam, R.V.S. Satyanarayana, "Gilbert Cell-Based Active Mixers: A Critical Study," IUP Journal of Telecommunications, Vol. 12, Issue 1, pp **25-45**, **2020**.

[11] W. Wang, Y. Xiong, B. Han, S. Feng and Y. Wang, "Design of a 3.1-10.6GHz CMOS Mixer for UWB Receiver," International Conference on Wireless Communications, Networking, Wuhan, China, **2011**.

[12] A.V. Padaki, R. Tandon and J. H. Reed, "On Adjacent Channel Co-Existence with Receiver Nonlinearity," in IEEE Transactions on Wireless Communications, Vol. **17**, No. **7**, **2018**.

[13] Avvaru Subramanyam, Satyanarayana RVS, "Noise Optimization and Linearization of RF Mixer using Inductive Peaking and Source Degeneration for Radio Local Area Network and Low Power Wireless Access Systems Applications," IEEE conference on VLSI SATA, Amrita School of Engineering, Bengaluru, **2022**.

[14] Wireless Planning and Coordination Wing, "National Frequency Allocation Plan- 2018", Ministry of Communications, Department of Tele-communications, Government of India, **2018**.

[15] Agilent Technologies, "Advanced Design Systems (ADS) Cook book", **2011**.

[16] Paynter, "Introductory Electronic Devices and Circuits: Conventional Flow," 7th Edition, Pearson Education, **2008**.

[17] W. Lee, K. Tsang, Y. Shen, K. Chui, A Current Bleeding CMOS Mixer Featuring LO Amplification Based on Current-Reused Topology, Circuits and Systems, Vol. **4**, No. **1**, **2013**.

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